UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,943	08/26/2003	Motomu Hashizume	TI-35328	3032

23494 7590 06/23/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
DAVIDSON, DAN	
ART UNIT	**PAPER NUMBER**
2627	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,943	HASHIZUME ET AL.	
	Examiner	Art Unit	
	Dan I. Davidson	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show a ground resistor 38 as described in the specification at paragraph 21. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claims 1 and 13; the specification never states that the biasing loop is a constant-voltage and constant-current biasing loop. The main embodiment of the specification uses a constant-voltage biasing loop. The specification at paragraph 23 discloses that a constant-current biasing loop may be used as an *alternative* to a constant-voltage biasing loop (emphasis added). Moreover, the use of a constant voltage across the MR head and a constant current through the MR head would result in a constant resistance across the MR head and would thus make the circuit inoperable. Accordingly, for the purposes of examination, the Examiner will read the limitation drawn to a constant-voltage and constant-current biasing loop as drawn simply to a constant-voltage biasing loop since doing so is consistent with the main embodiment of the specification. Claims 2-12 and 14-15 are respectively rejected as being dependent on claims 1 and 13, respectively.

Re claims 2-3; the Applicant never discloses in the specification that the common-mode feedback circuit comprises first and second current sources respectively coupled to first and second terminals of the MR head.

Re claim 4; the specification provides that the reference current source (Figs. 1 and 2, 28) is coupled between the emitter of transistor Q3 (or Q4) and a bottom rail, not between the central node and a bottom rail.

Re claims 5 and 13; the specification provides that the third bipolar transistor Q3 (claim 5, lines 8-9) is coupled to a bottom rail (i.e. ground) directly, not via a resistor. Furthermore, the central node (claim 5, lines 17-19) is not operatively coupled between a base of the fourth bipolar transistor, and the first and second terminals of the MR head; rather, the central node is coupled between a base of the fourth bipolar transistor and a stabilizing network comprised of resistors 34 and 36.

Re claims 6-7, 11-12, and 14-15; the bipolar transistors cannot comprise JFETs and MOSFETs, since JFETs and MOSFETs are both field-effect transistors, not bipolar transistors. When paragraph 11 of the specification states that "[p]referred embodiments of the invention may be implemented using either MOSFETs or JFETs," it must of necessity be speaking about using the above transistors as an alternative to using bipolar transistors.

Re claims 10 and 13; the base of the sixth bipolar transistor Q6 (claim 10, lines 10-11) is not operatively coupled to the MR head; rather, it is operatively coupled to transistor Q20. Likewise, the base of the fifth bipolar transistor Q5 (claim 10, lines 13-14) is not operatively coupled to the MR head; rather, it is operatively coupled to transistor Q22.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims are indefinite since the independent claims contain language not enabled by the specification. See above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Jove et al (US 5,204,789 A).

Re claim 1; Jove et al disclose an MR head biasing circuit (Fig. 2; column 3, lines 36-37) comprising: an MR head (Fig. 2, 11); a constant-voltage biasing loop (Fig. 2, 14; column 3, lines 29-37); and a common-mode feedback loop (Fig. 2, 15; column 4, lines 51-52) operatively coupled to the MR head and the constant-voltage biasing loop (see Fig. 2) for maintaining the MR head potential at approximately zero Volts (column 4, lines 51-56; column 7, lines 3-11; col. 1, lines 23-24 (the disk is typically grounded)).

Re claims 16-17; Jove et al disclose providing constant-voltage biasing to an MR head subcircuit (Fig. 2, 14; col. 3, lines 29-37); mirroring the current in a common-mode feedback circuit and substantially eliminating any current differential (col. 4, line 65 – col. 5, line 4); thereby maintaining the potential difference at the MR head to

approximately zero Volts (col. 4, lines 51-56; column 7, lines 3-11; col. 1, lines 23-24). Jove et al further disclose the step of providing reference current to the common-mode feedback subcircuit (Fig. 2, Jff4, Jff3).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shinohara (US 5,831,783 A) teaches providing a reference voltage from a signal processing circuit to a magnetic head for setting the head at an intermediate electric potential between a positive source voltage and a negative source voltage supplied by a power source unit.

Smith (US 5,327,303 A) teaches a circuit that protects MR elements from short circuits of the disk medium.

Jove et al (US 4,879,610 A) teach maintaining the center potential of an MR element to a selected reference voltage to protect the MR element from short circuits to a conductive area of a magnetic recording medium.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan I. Davidson whose telephone number is (571) 272-7552. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea L. Wellington, can be reached on (571) 272-4483. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DID
Dan I Davidson
June 13, 2006

ANDREA WELLINGTON
SUPERVISORY PATENT EXAMINER